Claims

[c1] An optical sensor package comprising:
a chip carrier;
a device chip electrically and mechanically connected to a first surface of the chip carrier with solder connections, the device chip having an optical sensing element on a surface thereof;
a capping chip secured to the chip carrier to hermetically enclose the device chip, the capping chip having means for enabling radiation to pass through the capping chip to the device chip;
conductive vias electrically connected to the solder connections of the device chip, the conductive vias extending through the chip carrier from the first surface thereof to a second surface thereof; and
bond pads on the second surface of the chip carrier and electrically connected to the conductive vias.

[c2] The optical sensor package according to claim 1, wherein the chip carrier is formed of a low-temperature co-fired ceramic material.

[c3] The optical sensor package according to claim 1, wherein the device chip is received in a recess formed in the chip carrier.

[c4] The optical sensor package according to claim 1, wherein the means for enabling radiation to pass through the capping chip comprises a monocrystallographic silicon portion of the capping chip.

[c5] The optical sensor package according to claim 4, wherein the means for enabling radiation to pass through the capping chip further comprises an antireflection coating on a surface of the capping chip and overlying the monocrystallographic silicon portion thereof, the antireflection coating minimizing reflection of a range of radiation wavelengths by the capping chip.

[c6] The optical sensor package according to claim 4, wherein the means for enabling radiation to pass through the capping chip further comprises a coating on a surface of the capping chip, the coating being substantially opaque to a range of radiation wavelengths and having an opening aligned with the

monocrystallographic silicon portion of the capping chip and the optical sensing element on the device chip.

[c7] The optical sensor package according to claim 1, further comprising a substrate having conductors on a surface thereof, and solder connections securing the package to the substrate and electrically and mechanically connecting the bond pads on the second surface of the chip carrier to the conductors on the substrate.

[c8] The optical sensor package according to claim 1, wherein the chip carrier is one of a plurality of chip carriers defined by a chip carrier wafer, the capping chip is one of a plurality of capping chips defined by a capping chip wafer, and the device chip is one of a plurality of device chips enclosed between the chip carrier wafer and the capping chip wafer.

[c9] An infrared sensor package comprising:
a chip carrier formed of a low-temperature co-fired ceramic material, the chip carrier having a first surface, an oppositely-disposed second surface, conductive vias extending through the chip carrier between the first and second surfaces thereof, and bond pads on the second surface and electrically connected to the conductive vias;
a device chip flip-chip mounted to the first surface of the chip carrier with first solder connections electrically connected to the conductive vias of the chip carrier, the device chip having an infrared sensing element on a surface thereof; and
a capping chip secured with a solder ring to the chip carrier to hermetically enclose the device chip within a cavity defined between the chip carrier and the capping chip, the capping chip being formed of monocrystallographic silicon so as to enable infrared radiation to pass through a wall portion of the capping chip to the infrared sensing element on the device chip, the solder ring having a lower melting temperature than the first solder connections.

[c10] The infrared sensor package according to claim 9, further comprising an antireflection coating on a surface of the capping chip and overlying the wall portion thereof, the antireflection coating minimizing reflection of infrared

radiation by the capping chip.

[c11] The infrared sensor package according to claim 9, further comprising a coating on a surface of the capping chip, the coating being substantially opaque to infrared radiation and having an opening aligned with the wall portion of the capping chip and the infrared sensing element on the device chip.

[c12] The infrared sensor package according to claim 9, further comprising a substrate having conductors on a surface thereof, and second solder connections securing the package to the substrate and electrically and mechanically connecting the bond pads on the second surface of the chip carrier to the conductors on the substrate, the second solder connections having a lower melting temperature than the first solder connections and the solder ring.

[c13] The infrared sensor package according to claim 9, wherein the chip carrier is one of a plurality of chip carriers defined by a chip carrier wafer formed of the low-temperature co-fired ceramic material, the capping chip is one of a plurality of capping chips defined by a capping chip wafer formed of monocrystallographic silicon, and the device chip is one of a plurality of device chips enclosed between the chip carrier wafer and the capping chip wafer.

[c14] A method of fabricating an optical sensor package, the method comprising the steps of:

forming a chip carrier to have conductive vias that extend through the chip carrier from a first surface thereof to a second surface thereof;

securing a device chip to the first surface of the chip carrier with solder connections that electrically connect the device chip to the conductive vias of the chip carrier, the device chip having an optical sensing element on a surface thereof; and

securing a capping chip to the chip carrier to hermetically enclose the device chip, the capping chip having means for enabling radiation to pass through the capping chip to the device chip.

[c15] The method according to claim 14, wherein the chip carrier is formed of a low-

temperature co-fired ceramic material, and the conductive vias are formed by screen printing during a green tape portion of forming the chip carrier.

[c16] The method according to claim 14, wherein the chip carrier is formed of a low-temperature co-fired ceramic material, and the device chip is placed in a recess formed in the chip carrier.

[c17] The method according to claim 14, wherein at least a portion of the capping chip is formed of a monocrystallographic silicon to enable radiation to pass through the capping chip.

[c18] The method according to claim 17, further comprising the step of forming an antireflection coating on a surface of the capping chip and overlying the monocrystallographic silicon portion thereof, the antireflection coating minimizing reflection of a range of radiation wavelengths by the capping chip.

[c19] The method according to claim 17, further comprising the steps of forming a coating on a surface of the capping chip, the coating being substantially opaque to a range of radiation wavelengths and having an opening aligned with the monocrystallographic silicon portion of the capping chip and the optical sensing element on the device chip.

[c20] The method according to claim 14, further comprising the step of securing the package to a substrate with solder connections that electrically connect the conductive vias of the chip carrier to conductors on the substrate.

[c21] The method according to claim 14, wherein the chip carrier is one of a plurality of chip carriers defined by a chip carrier wafer, the capping chip is one of a plurality of capping chips defined by a capping chip wafer, and the device chip is one of a plurality of device chips enclosed between the chip carrier wafer and the capping chip wafer, and wherein the step of securing the capping chip to the chip carrier comprises securing the capping chip wafer to the chip carrier wafer to form a wafer stack, the method further comprising the steps of performing automated simultaneous testing of the device chips; and then singulating the wafer stack to separate the package.

[c22] A method of simultaneously fabricating a plurality of infrared sensor packages, the method comprising the steps of:
forming a chip carrier wafer of a low-temperature co-fired ceramic material, the chip carrier wafer comprising a plurality of chip carriers, each chip carrier having a first surface, an oppositely-disposed second surface, conductive vias extending therethrough between the first and second surfaces, and bond pads on the second surface and electrically connected to the conductive vias, the conductive vias being formed by screen printing during a green tape portion of forming the chip carrier wafer;
flip-chip mounting a device chip to the first surface of each chip carrier, the device chip being mounted with first solder connections that electrically connect the device chips to the conductive vias of the chip carriers, the device chip having an infrared sensing element on a surface thereof;
securing a capping chip wafer to the chip carrier wafer with solder rings to form a wafer stack, each of the solder rings hermetically enclosing a corresponding one of the device chips within a cavity defined between their respective carrier and capping chips, the capping chip wafer being formed of monocrystallographic silicon so as to enable infrared radiation to pass through a wall portion of each capping chip to each of the device chips, the solder rings having a lower melting temperature than the first solder connections;
performing automated simultaneous testing of the device chips; and then
singulating the wafer stack to separate the plurality of infrared sensor packages.

[c23] The method according to claim 22, further comprising the step of applying an antireflection coating to a surface of the capping chip and overlying the wall portion thereof, the antireflection coating minimizing reflection of infrared radiation by the capping chip.

[c24] The method according to claim 22, further comprising the step of applying a coating on a surface of the capping chip, the coating being substantially opaque to infrared radiation and having an opening aligned with the wall portion of the capping chip and the infrared sensing element on the device chip.

[c25] The method according to claim 22, further comprising the step of securing the

packages to substrates with second solder connections that electrically connect the conductive vias of the chip carriers to conductors on the substrates, the second solder connections having a lower melting temperature than the first solder connections and the solder rings.